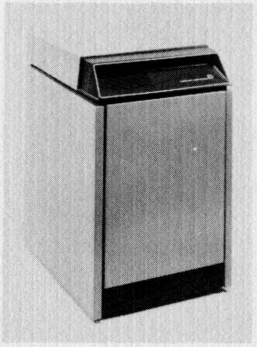
DATAPOINT
Product Specifications

67 and 135 MB Disk Drives

9395/9397/9331 /9332/9333



The 67 and 135 MB Disk Drive

April 24, 1981 Document No. 61036

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1.0 General Description

The Datapoint® 9395 and 9332 Dual Disk Drives provide Datapoint's 8800 processor with extensive random access mass storage capability. The 9395 Dual Disk Drive is the minimum system for the 8800 and consists of a 67 MB removable disk and a 135 MB non-removable disk for 202 MB of formatted on-line storage. For 8800 users with larger storage needs, the 9332 Dual Disk Drive furnishes two 135 MB non-removable disks totaling 270 MB of formatted storage capacity. As processing and storage needs grow, users may need to expand their disk configurations. The 9331 Single Disk Drive contains one 135 MB non-removable disk in a cabinet with space available for another. The 9333 Expansion Drive is a 135 MB non-removable disk without a cabinet intended as an addition to the 9331. For those who did not initially order disks with the 8800 processor, the 9397 Dual Disk Drive contains a 67 MB removable disk, a 135 MB non-removable disk, and a disk controller interface module (IMOD) for the 8800 processor. (See Section 1.1 for model codes and brief descriptions.)

The operation procedures for the 67 MB and the 135 MB disks are the same for all the disk drive models. However, for the purpose of simplicity this document will refer to all of the disk drives (single and dual) as the 67 MB/135 MB Disk Drives.

The disk drives interface to a controller board inside the 8800 processor. The controller can support up to four dual disk drives or eight single disk drives in any mix through daisy-chain connections. Data can be transferred to or from the main memory using up to four word multiple cycle transfers.

The disk drives are housed in a freestanding cabinet similar in styling and design to the cabinet holding the 8800 processor.

1.1 Model Code Descriptions

9331	Single Disk Drive 135 MB non-removable disk (in cabinet with space for 9333 expansion drive)
9332	Dual Disk Drive two 135 MB non-removable disks (in cabinet)
9333	Expansion Drive 135 non-removable disk (without cabinet)
9395	Dual Disk Drive, 67 MB removable disk, 135 MB non-removable disk (in cabinet)
9397	Dual Disk Drive, 67 MB removable disk, 135 MB non-removable disk (in cabinet), Disk Controller IMOD for 8800 processor

NOTE: The 9397 Dual Disk Drive is intended only for those who did not initially order the disk IMOD with the 8800 (Model 8830) processor.

2.0 Disk and Controller Configuration

The 67 MB/135 MB Disk Drives interface to the controller module via a standard Datapoint interface. The disk controller occupies two board locations in the 8800 chassis. The interface to the disk drive is provided through two cables, an 'A' cable for control signals and a 'B' cable for data and clock signals.

2.1 Interface Descriptions

The interfaces to the disk controller consist of the Disk interface, the Memory Bus interface and the Peripheral Control Bus interface.

2.1.1 Disk Interface

The 67 MB/135 MB Disk Drives have an 'A' cable which may be daisy chained to other drives and a 'B' cable which is connected directly to each individual drive. The disk drive cables connect to a disk I/O interface panel at the rear of the 8800 chassis. This panel can accommodate one 'A' cable and up to four 'B' cables. A disk I/O interface extention panel (Model Code 8891) is also available to accommodate up to four additional 'B' cables, which allow interfacing a maximum of eight drives.
All internal cables go to the disk controller board. Differential line drivers and receivers are used in the transmission of signals over the 'A' and 'B' cables. Refer to Section 6.0 for the cable connector pin assignments.

2.1.2 Memory Bus Interface

The Direct Memory Access (DMA) logic in the controller transfers data via the memory bus to or from the 8800 memory in one, two, three or four word bursts. The number of transfers done is controlled by the Arithmetic/Logic Unit (ALU) based on need. The DMA logic is designed to make transfers over the full 22 bit DMA absolute address range.

2.1.3 Peripheral Control Bus Interface

The Peripheral Control Bus Interface contains all of the logic necessary to establish communication between the controlling processor and the disk controller. All commands are taken via this logic, and all required status is returned to the controlling processor upon completion of a command.
Part of the interface contains the logic for the generation of vectored interrupts. This logic consists of a Z80-CTC peripheral chip with associated circuitry. The chip may be programmed by the controlling processor to monitor the interrupt conditions described in Section 3.7.

3.0 Technical Description

3.1 Technical Specifications

3.1.1 Disk Capacity (for both drives unless noted)

Bit Density	
67MB	6220 BPI (inner track)
135 MB	6038 BPI (inner track)
Track Density	
67MB	384 TPI
135 MB	680 TPI
Bit Transfer Rate	9.677 MHz
Byte Transfer Rate	1.209 MHz

3.1.2 Disk Timing Characteristics

Rotation	3600 RPM
Average Rotational Delay	8.33 milliseconds
Head Positioning	
Average	30 milliseconds
Maximum	55 milliseconds

67 and 135 MB Disk Drives

9395/9397/9331 /9332/9333

Continued....

3.1.3 Disk Format (for each drive unless noted)

Surfaces	8
Cylinders	823
Tracks/Cylinder	
67 MB	5
135 MB	10
Sectors/Track	
67 MB	64
135 MB	*66
Bytes/Sector	
67 MB	315
135 MB	305 for 65 sectors, 335 for last (66) sector
Bytes/Track	16,384
Bytes/Pack	
67 MB	67,420,160 (formatted)
135 MB	134,840,320 (formatted)

* Two sectors are used as spare areas on the disk. Because the 135 MB disk is not removable, these two spare sectors are used to replace bad sectors if the media is damaged.

3.2 Operator Controls and Indicators

The indicator panels are located on the inside panel of the dual disk drive cabinet. To gain access to the switch/indicator panels, open the cabinet door from the right front edge. The switch/indicator panels will appear as in Figures 3-1 or 3-2 for the removable and non-removable disks, respectively. The indicator panels of the removable and non-removable disk drives differ slightly in appearance, although they operate in essentially the same way.

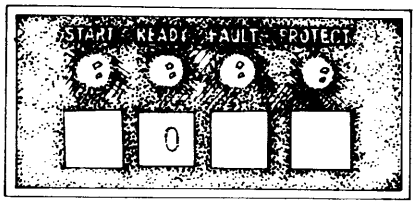


Figure 3-1. Switch/Indicator Panel for Removable Disk Drive

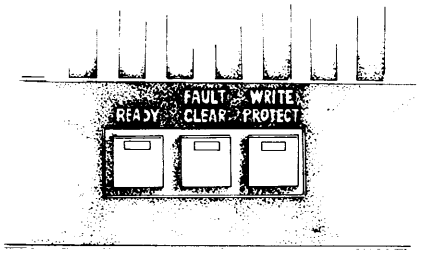


Figure 3-2. Switch Indicator for Non-removable Disk Drive

3.2.1 Removable disk switch/indicator panel (upper drive)

START Switch/Indicator — The START switch/indicator starts and stops the spinning of the drive spindle. To start the drive, press the switch and the indicator will light. To stop the drive, press the switch and the drive will power down.

READY Indicator — The READY indicator starts flashing when a start or stop cycle is in progress. When a start cycle has been completed, the READY indicator will stop flashing and remain lit. When a stop cycle has been completed, the indicator will stop flashing and go dark.

FAULT Switch/Indicat — When the FAULT indicator lamp is lit, a fault condition has been cleared, the indicator may be reset by pressing the fault switch again. If the fault indicator does not go out (indicating that the fault condition cannot be cleared), contact a Datapoint Customer Service Representative.

PROTECT Switch/Indicator — The PROTECT switch/indicator lets you inhibit the writing of data to the disks. When the PROTECT indicator is off, data may be written on the disk. To write protect the disk, press the PROTECT switch until it latches and the PROTECT indicator comes on. When the indicator is on, no data may be written on the disk. When you are ready to write to the disk again, press the switch until it unlatches and the indicator light goes out.

3.2.2 Non-removable disk switch/indicators (lower drive)

READY Indicator — The READY indicator starts flashing when a start or stop cycle is in progress. When a start cycle has been completed, the indicator will stop flashing and remain lit. When a stop cycle has been completed, the READY indicator will stop flashing and go dark.

FAULT CLEAR Switch/Indicator — When the FAULT CLEAR indicator light is lit, a fault condition exists. After the fault condition has been cleared, the indicator may be reset by pressing the FAULT CLEAR switch. If the fault indicator does not go out (indicating that the fault condition cannot be cleared), contact a Datapoint Customer Service Representative.

WRITE PROTECT Switch/Indicator — The WRITE PROTECT switch inhibits the writing of data to the disk. When the WRITE PROTECT indicator is off, data may be written on the disk. To write protect the disk, press the WRITE PROTECT switch until it latches and the indicator light comes on. When the indicator is on, no data may be written to the disk. When you are ready to write to the disk again, press the switch until it latches and the indicator light will go dark.

3.3 Disk Pack Loading

Upper Drive (67 MB only)

Pull the disk cabinet door open from the right front edge to expose the removable disk drawer on the upper drive. The removable disk drawer is shown in Figure 3-3.

With the READY and START indicators off, slowly slide out the removable disk drawer by pressing the drawer release latches on either side of the drawer at the bottom, and pulling the drive drawer out as far as possible.

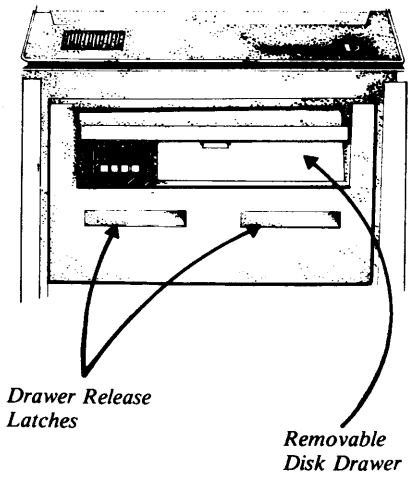


Figure 3-3. Removable disk drawer in cabinet

When the drawer has reached its full extension, release the cover latch in the front center of the cover (see Figure 3-4) and raise the cover up as far as possible.

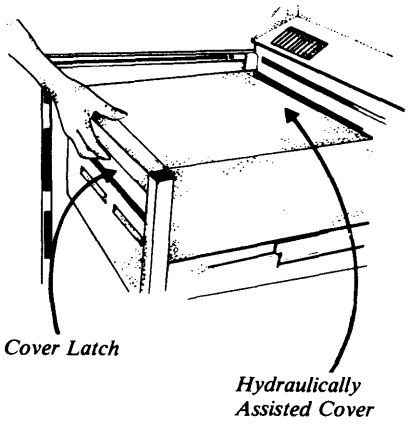


Figure 3-4. Releasing cover latch

Lifting and holding the removable disk pack by its handle, release its bottom cover by pressing together the two semicircular grips; remove the bottom cover. Carefully lower the disk pack onto the drive spindle until it rests in position. The fit of the disk pack inside the enclosure is snug, so be sure to lower the disk pack straight onto the spindle and turn the handle clockwise until it stops in order to seat the pack in the drive.

Remove the top cover of the disk pack by rotating it approximately three clockwise turns until a clicking sound is heard. The cover will come free and may be lifted off.

Close the hydraulically assisted drive cover until you hear a sharp snap as its latch engages. Push the drive drawer back into the cabinet until both drawer release latches snap closed.

Press the START switch to begin the start cycle. The drive will be up to speed in about twenty seconds, and the ready indicator will stop flashing and remain lit. Close the cabinet door, and the disk drive will be ready for operation. Figure 3-5 illustrates the proper procedure for loading a disk pack.

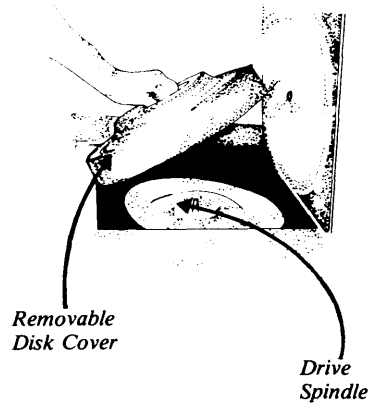
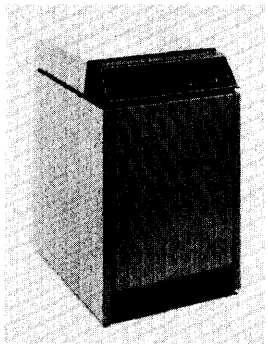


Figure 3-5. Loading a removable disk pack



67 and 135 MB Disk Drives

9395/9397/9331 /9332/9333

3.4 Disk Pack Unloading

Upper Drive (67 MB only)

Unloading the disk pack from the drive is done in the same sequence as loading, but in the reverse order:

Open the front cabinet door from the right edge. With the indicator lamp lit, press the START switch and the stop cycle will begin. The START light will go out and the READY indicator will flash.

After about twenty-five seconds, the disk pack will have stopped spinning, and the READY indicator will stop flashing and go dark.

Next, press the drawer release latches inside the grips on either side of the drawer at the bottom, and pull the drawer out as far as possible. Release the cover latch and raise the cover up as far as possible.

Hold the disk pack cover by the handle and carefully lower it over the disk pack until it will go no further, then rotate the cover approximately three full turns counter clockwise until you hear a clicking sound.

The entire disk pack and cover may then be lifted off the drive spindle and out of the drive. You should immediately replace the bottom cover of the pack.

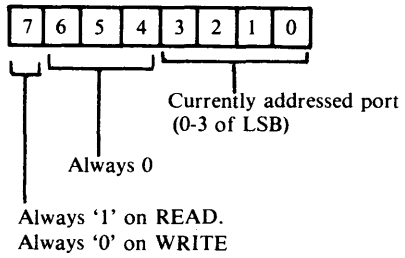
3.5 Disk Control and Status Registers

There are three ports in the disk controller. The various registers set in each port are used to accept command parameters, return status and generate appropriate interrupts. The following subsections describe the ports, the registers and the meaning of each bit in these registers.

3.5.1 Port 0 Registers

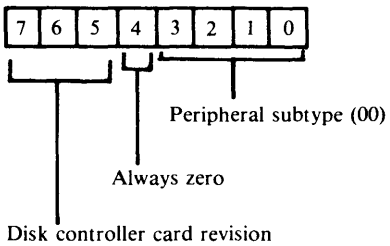
3.5.1.1 Register 0 - Base Register

The Base Register is written to address a new port in the disk controller. This register is read to determine the currrently addressed port. The format of the base register is as follows:



3.5.1.2 Register 1 - I.D. Register

The I.D. Register is a read only register. This register may be read by performing an I/O read to register 1. There is only one ID register. The four LSB bits of the ID register are used to categorize the IMOD into 16 subtypes. The purpose for sub-types is to differentiate between IMOD types which interface to functionally different peripherals of the same class. The disk controller has a peripheral subtype of 00. The three MSB bits of the I.D. Register contain the version level of the disk IMOD and are available for future revision levels in expanded configurations. The ID register byte format is as follows:



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3.5.1.3 Register 2 - Disk Parameter Buffer

The Disk Parameter Buffer is a four deep register file and must be accessed four times whenever a write is performed. The bit configuration of each byte is below:

Byte	Bits	Meaning
0	0,1	Cylinder MSB bits
	2-7	Track error information (indicating the number of consecutive sectors available following and including sector 0)
1	0-7	Cylinder LSB bits
2	0-3	Head Number
	4	Drive type (1 for the non-removable drive, and 0 for the removable drive)
	5,6	Number and distribution of defects in this track
	7	Bit set to 1 to indicate a defective track
3	0-6	Starting logical sector address, except on a read header command
	7	Always 0, except for the read header command

The bit configuration of the Disk Parameter Buffer is illustrated below:

Byte#	Bit# 7	6	5	4	3	2	1	0
0	T	T	T	T	T	T	C9	C8
1	C7	C6	C5	C4	C3	C2	C1	C0
2	T	T	T	D	H3	H2	H1	H0
3	0	S6	S5	S4	S3	S2	S1	S0

Where:

T = Track Error Information (Refer to Section 3.8.2 for a detailed description of the error information)
Cx = Cylinder Number
Hx = Head Number
Sx = Starting Sector Address
D = Drive Type

3.5.1.4 Register 3 - Disk Address Buffer

The disk address buffer is a write only four deep register file. It contains the DMA address pointer in a seek interrupt mask.

Byte	Bit	Meaning
0	0-4	MSB of the DMA address right shifted one place
	5-7	Always zero
1	0-7	DMA address middle byte right shifted one place
2	0-7	DMA address middle byte right shifted one place
3	0-7	Not used, always 0

The bit configuration of the Disk Address Buffer is illustrated below:

Byte#	Bit# 7	6	5	4	3	2	1	0
0	0	0	0	MA 21	MA 20	MA 19	MA 18	MA 17
1	MA 16	MA 15	MA 14	MA 13	MA 12	MA 11	MA 10	MA 9
2	MA 8	MA 7	MA 6	MA 5	MA 4	MA 3	MA 2	MA 1
3	NU	NU	NU	NU	NU	NU	NU	NU

Where:
MAx = Starting DMA address right shifted one place
NU = Not used, always 0
Note: LSB of starting DMA address is always 0

3.5.1.5 Register 4 - Sector Counter

Register 4 can be read by the processor at any time. It contains the current sector number selected. If no unit is selected, this register will contain no relevant information.

Bits 0-6
Present value of the sector corresponding to the unit that is currently selected.

Bit 7
If this bit is set, the value contained in bits 0 through 6 is valid. If this bit is 0, the sector counter is not in sync with the actual sector value.

The format of the bits in the Sector Counter Register is illustrated below:

Bit# 7	6	5	4	3	2	1	0
OK	N6	N5	N4	N3	N2	N1	N0

Nx = Current Sector #

3.5.1.6 Register 5 - Command

The command buffer is a write only register containing the preassigned command codes for the disk controller. Any code other than the ones assigned will result in an illegal command status returned in Port 1, Register 2, Byte 2, Bit 2.

The assigned command codes in octal are as follows:
Normal Read - 0200
Normal Write - 0201
Write 135 MB - 0220
Format - 0202
Seek - 0203
Drive Select - 0204
Fault Clear-0205
Read Header - 0206
Normal Read, Data Strobe Normal, Offset Normal - 0207
Read With Data Strobe Early, Servo Normal - 0257
Read With Data Strobe Late, Servo Normal - 0247
Read With Strobe Normal, Offset Plus - 0327
Read With Strobe Normal, Offset Minus - 0307
Read With Strobe Early, Offset Plus - 0377
Read With Strobe Early, Offset Minus - 0357
Read With Strobe Late, Offset Plus - 0367
Read With Strobe Late, Offset Minus - 0347
Configure Drive Type - 0210
Read Record Using Sector Counter - 0214
Write Record Using Sector Counter - 0213
Verify - 0221
Long Read - 0211
Long Write - 0212
Controller Reset - 0216
Drive Reset (return to zero) - 0217
Align Heads - 0223

The figure below illustrates the bit configuration in the Command Buffer byte.

Bit#	7	6	5	4	3	2	1	0
	CMMD OK	CMD 6	CMD 5	CMD 4	CMD 3	CMD 2	CMD 1	CMD 0

Where:
CMDx = Command Code CMMD OK = Command Valid

3.5.1.7 Register 6 - Unit Buffer

Register 6 is a write only four deep register file containing information about the unit number and number of sectors to read or write. One byte of this register file is reserved for future expansion and must be coded as zero.

Byte	Bit	Meaning
0	0-5	Number of sectors or read/write
	6,7	Always zero
1	0-4	Always
	5-7	Unit number
2	0-7	Zero to enable boundary checks on parameters
3	0-7	Always zero

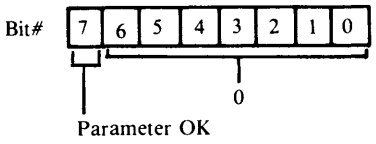
The bit configuration of the Unit Buffer is illustrated below:

Byte# \ Bit#	7	6	5	4	3	2	1	0
0	0	0	SC 5	SC 4	SC 3	SC 2	SC 1	SC 0
1	U2	U1	U0	0	0	0	0	0
2	N	N	N	N	N	N	N	N
3	NU	NU	NU	NU	NU	NU	NU	NU

Where:
SCx = Number of sectors to read or write
Ux = Unit number
N = Zero to enable boundary checks on parameters
NU = Not Used

3.5.1.8 Register 7 - Parameter OK Buffer

Register 7 is a write only register, and writing is allowed only to bit 7. This bit is set by the controlling processor to indicate that a valid set of parameters is available to the disk controller through other registers of this port. Upon finding this bit set, the controller will accept the parameters, generate a suitable interrupt and reset this bit. Bit 7, whether accepted or not, can be found by the processor by reading Port 1, Register 5, Bit 7. The figure below illustrates the bit configuration in the Parameter OK Buffer:



3.5.2 Port 1 Registers

Port 1 contains registers carrying information about the last operation performed, and whether or not the disk controller will accept a new command. This bit, accepted or not, can be found by reading Port 1, Register 5, bit 7.

3.5.2.1 Register 2 - Error Status Buffer (Read Only)

Register 2 is a four deep register file. The bytes and bits and their meanings are described in the sections below.

Byte 0
Bit 0 - FIFO Error
When this bit is set during a read operation, a FIFO underrun or overrun has occurred and the transferred data is probably in error. When this bit is set during a format operation, one of the following conditions exists:

- Actual FIFO underrun/overrun condiions
- DMA rate error has occurred causing a FIFO error

Continued....

In any case the data written in the record is in error and must be rewritten.

Bit 1 - Memory Error
An uncorrectable memory error has occurred during a DMA transfer.

Bit 2 - Busy
The controller is busy and will not accept any command except CONTROLLER RESET.

Bit 3 - ECC Error
An ECC error has occurred during a read.

Bit 4 - EP Valid
During an error recovery operation, a valid pattern for the ECC Error bit (bit 3) is available through PORT 1, Register 3. If this bit is not set during an error recovery operation, the ECC error encountered, if any, is one of an uncorrectable variety.

Bit 5 - Summary Error
An error condition was present during the last operation.

Bit 6 - Sync Lost
One of the following conditions exists:

- No valid sync pattern is written in the record that the controller last tried to read.
- During an actual read/write format, the read or the servo clock has been dropped.

Bit 7 - Multiple Sector Abort
A multiple sector operation has been aborted as a result of one of the following conditions:

- A fatal error was encountered. If the error was encountered in the last sector of a multiple sector operation, this bit will not be set.
- The controlling processor issued a control reset command during the execution of either a multiple sector operation or a single sector read recovery operation.

Byte 1

Bit 0 - Sector Not Found

When this bit is set one of the following conditions exists:

- During a write operation the target sector could not be found because either such a header doesn't exist or the record has an ECC error.
- During a multiple sector read operation, record N does not have the sector number equal to N-1 plus 1, and the multiple sector read has been aborted.

Bit 1 - Controller Time Out Error
The maximum time allowed by the controller to finish an operation is three seconds, following which the controller will set this bit and abort the operation.

Bit 2 - Illegal Command
The command given is not one of the assigned commands (Port 0, Register 5).

Bit 3 - Rate Error
If this bit is set during a DMA write operation, the 8800 memory failed to accept the data at a predetermined rate. During a DMA read (disk write) operation, failure by the memory to supply the data words when needed is reflected as a FIFO error.

Bit 4 - Sector Overrun
A sector or index pulse was detected before the reading, writing, or formatting of a record is finished.

Bit 5 - Not Used
Always zero

Bit 6 - Boundary Error
During the present command, one of the following error conditions has occurred:

- Head number given is greater than 4 or 11 if the drive type is 0 or 1, respectively.
- Unit number given is greater than 7.
- Starting sector number is greater than 77 for removable drives.

Bit 7 - Parameter Not Set
Within the allotted time, a set of parameters (either header or DMA address pointer or both) was not given by the controlling processor.

Byte 2

Bit 0 - Write Protected
The selected drive is write protected.

Bit 1 - Unit Ready
The selected drive is up to speed, on-line, and ready to accept commands.

Bit 2 - Seek Error
The selected drive has a seek error. The seek error must be cleared by either a return to zero command or by turning the DC power off and then on again.

Bit 3 - On Cylinder
The carriage assembly of the selected drive is stationary.

Bit 4 - Drive Fault
The selected drive has a fault condition present and must be cleared by using a FAULT CLEAR command or otherwise (manually) before this drive can be used again.

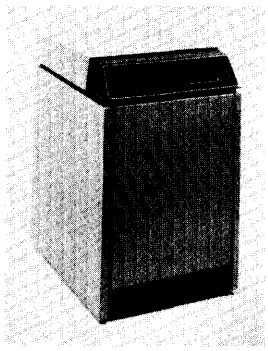
Bit 5 - Select Error
The unit to be selected is not on-line, or the unit to be selected is not the one requested. The operation is terminated.

Bit 6,7 - Not used
Always 0

Byte 3

Bits 0-7 - LSB bits of the error pattern
The bit configuration of the bytes in the Read Only Status Buffer are described in the figure below.

Byte# \ Bit#	7	6	5	4	3	2	1	0
0	MULT SECT ABORT	SYNC LOST	SUM ERROR	EP VALID	ECC ERROR	BUSY	MEM ERROR	FIFO ERROR
1	PARAM NOT SET	BOUND ERROR	0	SECT OVRUN	RATE ERROR	ILLEG CMD	TIME OUT ERROR	SECT NOT FOUND
2	0	0	SEL ERROR	DRIVE FAULT	ON CYL	SEEK ERROR	UNIT READY	WRITE PROT
3	SEEK END 7	SEEK END 6	SEEK END 5	SEEK END 4	SEEK END 3	SEEK END 2	SEEK END 1	SEEK END 0



67 and 135 MB Disk Drives

9395/9397/9331 /9332/9333

3.5.2.2 Register 3 - ECC Pattern Buffer (Read Only)

The ECC Pattern Buffer is a 4 deep register file and must be accessed four times (all 4 bytes) whenever a single byte is accessed. The bytes of this register contain information about the pointer and the pattern of the read data. The address pointer supplied is 11 bits long, and the pointer counting starts at 0.

Byte 0

Bits 0, 1, 2, 3
MSB four bits of the address pointer (bit displacement count).

Bits 4 - 7 are always zero.

If the error occurs in the first eleven bits of the header, Byte 0 and Byte 1 will contain a negative number. For example, if the error is in bit 0 (first header bit), Byte 0 and Byte 1 will contain 0377 and 0366 respectively.

Byte 1

Bits 0 - 7
LSB eight bits of the address pointer (starting bit position of the supplied error pattern).

Byte 2

Bits 0, 1, 2
MSB three bits of the error pattern.

Bits 3 - 7
Always zero.

Byte 3

Bits 0 - 7
LSB bits of the error pattern.

The bit configuration of the ECC Pattern Buffer is illustrated below:

Byte # \ Bit #	7	6	5	4	3	2	1	0
0	0	0	0	0	D11	D10	D9	D8
1	D7	D6	D5	D4	D3	D2	D1	D0
2	0	0	0	0	0	P10	P9	P8
3	P7	P6	P5	P4	P3	P2	P1	P0

Where:
Dx = Bit displacement count
Px = Error pattern

3.5.2.3 Register 4 - Header Buffer (Read Only)

The Header Buffer is a four deep register file and must be accessed four times. The bytes of this register file contain the cylinder head and sector information of the last operation performed. If a multiple sector operation is terminated before the actual completion of the operation, this register will contain the last sector attempted in the read/write or error termination operation. The bytes of this register are described in the sections below.

Byte 0

Bits 0, 1
MSB bits of the cylinder number.

Bits 2 - 7
These bits appear as zero during normal read/write format. However, during a read header command, these bits will be the actual bits as recorded on the particular header requested.

Byte 1

Bits 0 - 7
Cylinder LSB bits.

Byte 2

Bits 0 - 3
Represents head number.

Bit 4
Represents drive type.

Bits 5 - 7
These bits normally appear as zero except during a read header operation when these bits will be the actual bits recorded in the disk at the indicated sector position.

Byte 3

Bits 0 - 6
These bits indicate the current sector number.

Bit 7
Always zero, except in a Read Header operation. The bit configuration of the Header Buffer is illustrated below:

Byte # \ Bit #	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	C9	C8
1	C7	C6	C5	C4	C3	C2	C1	C0
2	0	0	0	D	H3	H2	H1	H0
3	SA 7	SA 6	SA 5	SA 4	SA 3	SA 2	SA 1	SA 0

Where:
Cx = Current Cylinder Number
Hx = Current Head Number
SAx = Current Sector Number
D = Drive Type
Upon power up or following a configure command, byte 0, bit 7 will indicate the type of drive (1 for 135 MB, 0 for 67 MB).

NOTE: Refer to Section 3.8.2 for a more detailed explanation of the track error information on headers in defective sectors.

Continued....

3.5.2.4 Register 5 - Command Status Buffer (Read Only)

Bits 0 - 3
Always one.

Bits 4, 5
Always zero.

Bit 6 - Command OK
This bit indicates that the controller is ready to accept a new command. Upon power up, this bit is set at one. No command other than control reset should be given to the controller as long as this bit is 0. When this bit is reset, the controller is busy performing the previous command.

Bit 7 - Parameter OK
This bit will normally appear as zero. When the processor writes the MSB of Port 0, Register 7, this bit is set. This bit will be reset by the controller whenever the controller has accepted the supplied address or the header, or both. The address pointer or the disk parameter buffer (Port 0, Register 2, and Register 3) should not be altered by the processor whenever this bit is set.

The bit configuration of the Command Status Buffer is illustrated below:

Bit #

7	6	5	4	3	2	1	0
PARAM OK	CMD OK	0	0	1	1	1	1

The Parameter OK bit is reset by the controller and set by the processor. Whenever the controller can accept a new command, it will set the CMD OK bit. Bits 0, 1, 2, and 3 are always 1.

3.5.3 Port 2 Registers

This port contains the various interrupt channels for the CTC chip. The register description are described in the following subsections.

3.5.3.1 Register 4 - CTC Channel 0 (Read/Write)

An interrupt through this channel is generated whenever:
(a) An operation is successfully completed.
(b) An operation is aborted because of a fatal error.

3.5.3.2 Register 5 - CTC Channel 1

An interrupt through Channel 1 is generated whenever the disk controller needs an updated DMA address or a header, or both.

3.5.3.3 Register 6 - CTC Channel 2

An interrupt is generated through Channel 2 whenever a seek operation is completed on a drive.

3.5.3.4 Register 7 - CTC Channel 3

An interrupt is generated through Channel 4 under the following conditions:

- During a multiple sector long read, an ECC error is encountered.The header buffer will contain the information about the record in error.
- During a multiple sector READ HEADER command, each header is successfully read (with proper ECC check). An interrupt is generated through this channel, and the processor can inspect the header buffer for the header information just read.

3.6 Detailed Command Description

All commands given to the Disk Controller unconditionally select the proper unit and head if necessary. The format command performs the seek to the specified cylinder before writing the track headers and data.
During Read, Write or Read Header type commands, it is assumed that the carriage is already positioned over the target cylinder and no seek is necessary.
The following subsections describe the commands in detail. (Op codes are in octal notation)

3.6.1 Normal Read, Op Code 0200

The Normal Read command reads logical sectors 0 through 64 including wrap around if desired. The controller automatically skips over unidentifiable sectors and transfers the contents of each subsequent sector for as long as the logical records accessed are sequential and the controller does not have to skip more than 66 sectors to locate the next logical record.

The Normal Read command reads 256 bytes of data from the specified unit, head, cylinder and record number without selecting a new head when a sector boundary is reached.

If the parameter OK bit is set by the processor at command execution time, the controller generates an interrupt through channel 1 at every sector for as long as necessary to complete the operation. Upon finding this interrupt, the controlling processor must supply an updated DMA address pointer (absolute memory address right shifted one place) and notify the controller by setting the parameter OK bit. If an updated pointer is needed, the controlling processor must supply the necessary information within approximately 220 microseconds of receiving the Channel 1 interrupt.

However, if the processor does not set the parameter OK bit at the beginning, the memory transfers will be done in contiguous memory locations. No further intervention by the processor will be necessary.

If the parameter OK bit is needed by the controller and not set by the processor within 220 microseconds of the channel 1 interrupt, the multiple sector operation aborts and a channel 0 interrupt is generated.

3.6.2 Normal Write, Op Code 0201

The Normal Write command writes continuous records without requiring the processor to supply additional headers at every sector. The microcode updates and maintains all headers in a sequential manner until the operation is completed. Even though the headers are maintained by the microcode, the DMA address, if needed, must be supplied by the processor employing the conventional protocol defined in this document.

There is no restriction on wrap around writes. However, the controlling processor must maintain the integrity of the pack during the write. During the wrap around write, the microcode does not check the validity of the headers written.

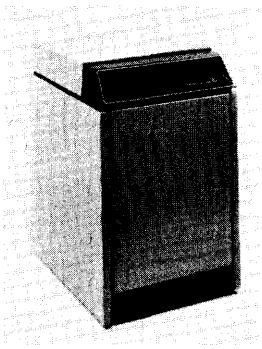
3.6.3 Write 135 MB Type, Op Code 0220

The Write 135 MB type writes up to a maximum of 66 sectors to the non-removable specified drive head and record number, provided such a header exists in the present track position. The initial DMA (Direct Memory Access) pointer must be supplied prior to initiating the write. During a multiple sector write operation, all records accessed must be under the present head. No new head will be selected if the last sector is reached and there are still more sectors to be written. If the previous condition occurs, records will be wrapped around and written over previously written data. The controlling processor must keep track of the starting and ending sector position during a write operation.

Initially, an attempt is made to locate the given target sector in the present track position. All header bits except the ten error information bits are read and compared against the supplied information. An interrupt is generated through channel 1 as the target sector search continues. When the processor finds this interrupt, it must supply the first header that is to be written following the target sector. If the data matches within one revolution of the disk pack, the ECC is verified. Writing begins on the next sector or index pulse if all of the above comparison is verified. If the comparison is not verified, the operation is aborted with a SECTOR NOT FOUND status posted and a channel 0 error interrupt.

Note that during this type of write operation, the processor must supply the header information to be written in the pack on every sector.

If the parameter OK bit was not set by the processor, the data that will be written in successive sectors will be picked up from contiguous memory locations. In a multiple sector operation, whether the parameter OK bit is set or not, after writing the first header the controller will reset the parameter OK bit and generate a Channel 1 Interrupt. The processor



67 and 135 MB Disk Drives

9395/9397/9331 /9332/9333

must supply an updated parameter OK bit set (header, memory address if any) within 210 microseconds. If the updated parameter OK bit is not supplied in the specified time, the PARAMETER OK NOT SET error status will be returned, a Channel 0 Interrupt will be generated, and the operation will be aborted.

If a power failure occurs during a write operation, the present sector is completely written to before the write operation is aborted.

3.6.4 Format Operaton, Op Code 0202

The Format command writes track headers for all possible sectors in the drive specified at the specified cylinder and head. Data for all records will be picked up from the same memory location. The Read Header buffer should contain the worst case data pattern as defined in Section 3.8.2. During a Format command, only one 256 byte buffer is needed to contain the worst case data pattern.

Since the headers are written from the header buffer, the controlling processor must supply all of the headers within the allotted time. If for some reason the format operation is aborted, the track will contain only partially formatted records. The track must be reformatted error-free before a Read operation can be performed on the track.

During a format operation, the controlling processor must supply all the necessary headers and the number of sectors to format at the time of execution of the command. Thus, it is possible to partially format a track. The reading ability of a partially formatted track cannot be guaranteed.

3.6.5 Seek, Op Code 0203

The Seek command allows the disk controller to issue a seek to the specified drive and cylinder.

The controller remains busy for approximately 15 microseconds. Seek Interrupts are generated whenever the seek is completed. Seek Interrupts are non-maskable; however, CTC channel 2 may be disabled when the Seek Interrupts are no longer needed.

If multiple Seek commands have been issued, and all the drives finish the Seek at the same time only one SEEK END interrupt will be generated through channel 2. The controlling processor can read the SEEK END status at any time. SEEK END interrupts are generated only at specific times, and therefore you may see a SEEK END status before the interrupt is generated.

3.6.6 Drive Select, Op Code 0204

The Drive Select command attempts to select the specified unit. Proper status is returned upon completion of the command. Drive Select may also be used to see if a particular unit exists in the system (during initial configuration time).

3.6.7 Fault Clear, Op Code 0205

This Fault Clear command unconditionally attempts to clear the fault condition on the specified drive. However, all fault conditions are not clearable using this command. Standard interrupt (busy to non-busy) is generated through channel 0.

3.6.8 Read Header, Op Code 0206

The Read Header command can be a single or multiple sector operation. It supplies the header information as recorded on the disk for the requested sector. The Read Header command can also verify the correctness of Error Correction Code written at the end of the record.

The Read Header command is the only command that will accept any physical number as the parameter for the operation. If byte 3, register 2, port 0 = 0377, the first good header found is returned, and the operation will continue until aborted. If byte 3, register 2, port 0 is not equal to 0377, the value given is used as a physical sector number. The header in that physical sector is read and returned. For all other commands, a logical sector address of 0376 (octal) or 0377 (octal) would be invalid and cause a boundary error.

During a multiple sector read operation, an interrupt through channel 3 is generated every time a header has been correctly read. The interrupt notifies the processor that the header bytes are available through the header buffer and that the header is good.

The Read Header operation begins whenever a good header is located. Normally a search is made to locate a good header with a try count of 66. As soon as a good header is found, an interrupt through channel 3 is generated. The reading of headers continues as long as such headers are available and the try count is non-zero.

It is the responsibility of the processor to terminate the Read Header operation either by a CONTROL RESET or by setting the Parameter OK bit. When the operation is terminated the controller is made non-busy, and no interrupt of any kind is generated. If the Read Header operation is started and not terminated by the processor within 67 good headers, the operation will abort with an error interrupt of SECTOR NOT FOUND. No special bit exists for this type of error interrupt.

3.6.9 Error Recovery/Error Pattern Search

The Error Recovery/Error Pattern Search command performs a single sector operation intended for recovering any data that is unrecoverable using conventional read methods. The record number read is the absolute physical record number present in the track. Therefore, if the track contains the logical record number, before issuing this command the controlling processor must make a physical to logical translation and supply that physical number as the target record number.

The Error Recovery/Error Pattern Search command allows the controlling processor to specify the read conditions such as read with carriage offset plus or minus, or read with data strobe early, late or normal. If an ECC error occurs during any of these read combinations, an automatic error pattern search is initiated. If the record can be read without an ECC error, no attempt is made to Error Pattern Search.

256 bytes of data will always be transferred during this group of commands. If an Error Patten Search has succeeded in finding a valid pattern, at the end of the search an 'EP VALID' status bit will be returned if the error is correctable along with the 'ECC ERROR' status bit. If the search has failed to locate the pattern, the operation will be completed with only the 'ECC ERROR' status bit returned.

Below are descriptions of all the possible command codes (in octal) for this group of read commands.

Op Code	Read Command
0207	Normal Read, Data Strobe Normal, Offset Normal
0257	Read with Data Strobe Early, Servo Normal
0247	Read with Data Strobe Late, Servo Normal
0327	Read with Strobe Normal, Offset Plus
0307	Read with Strobe Normal, Offset Minus
0377	Read with Strobe Early, Offset Plus
0357	Read with Strobe Early, Offset Minus
0367	Read with Strobe Late, Offset Plus
0347	Read with Strobe Late, Offset Minus

Continued....

If an ECC error is detected during any of the above read commands, an automatic search for an error pattern will be initiated. If the command is terminated with an 'EP VALID' status bit, then PORT 1 register 3 will contain two bytes of bit displacement in the error pattern (minimum 0, maximum 04120 [octal]) and two bytes (11 bits) of the error pattern. The first two bytes are the MSB bits and the lower eight LSB bits of the displacement. The third and fourth bytes will contain three MSB bits of the pattern and eight LSB bits of the pattern respectively.

If an error pattern search is initiated by the controller and the controller can find the specific pattern, the EP VALID and ECC ERROR will be posted generating a SUMMARY ERROR. (Such a condition is considered a normal completion.)

If the first 11 bits or any part thereof is in error, the supplied pointer in Bytes 0 and 1 will be a negative number. In order to correct such data, the supplied pattern should be left shifted the number of times corresponding to the number in the supplied data pattern. The resultant data pattern should be exclusive or'd with the given header starting at the MSB position of the header.

Note, the ECC search employed here will always be able to find one single occurrence of ten bits in error in a data stream. This search may also find an eleven bit error pattern, but it may or may not be a valid finding. The validity of the search depends on the number of bits in error within the eleven bit stream. For the specific layout of the bits see the register descriptions in Section 3.5.

3.6.10 Configure Drive, Op Code 0210

The Configure Drive command determines the type of drive, 67 MB or 135 MB. PORT 1, REG 4, BYTE 0 MSB bit will be returned as a 0 if it is a removable (67 MB) drive, or a 1 if it is a non-removable (135 MB) drive.

3.6.11 Read Record Using Sector Counter, Op Code 0214

The Read Using Sector Counter positions the target record by using sector pulses. During a multiple sector read, record N+1 is read and compared with N+1 where N is the previous record number read. If the current record does not compare to the previous record number plus 1, a maximum of 66 sectors will be skipped in an effort to locate the desired record. If the record cannot be located, the operation is terminated and a SECTOR NOT FOUND status is returned.

This operation is identical to a Normal Read operation except that in a Read Using Sector operation no header comparison is made on the first sector read. All error and other status returned is the same as a Normal Read.

Note that the first sector read of a multiple sector operation will be read using this type of positioning method. All the subsequent records are read using conventional positioning methods.

3.6.12 Write Record Using Sector Counter, Op Code 0213

The Write Using Sector Counter command is similar to the Read Using Sector Counter command, except that the Write command makes no comparison to determine whether or not the carriage is positioned over the appropriate cylinder. Since there is no comparison made, this command provides a means of writing to sector N if sector N-1 is bad.

The Write Using Sector Counter command positions the first record using sector pulses and writes the header and data at the sector positioned.

DMA transfers during multiple sector writes are from contiguous memory locations if the parameter OK bit is not set at execution time. After the controller writes the first header, it will generate a channel 1 interrupt if this is a multiple sector operation. Otherwise, a normal channel 0 interrupt is generated to mark the completion of the command.

During a multiple sector write, the processor must supply the new set of header bytes and DMA address pointer, if applicable, within 210 MS upon receipt of the interrupt through channel 1. If headers are not supplied within the allotted time, the operation is aborted with a channel 0 interrupt and a PARAMETER NOT SET error status is returned. Writing can be wrapped around; however, the processor must maintain the validity of the headers written as records are wrapped around.

3.6.13 Verify, Op Code 0221

The verify command verifies the ECC on records starting at a given logical sector number for as many as 64 sectors. If the number of headers specified can be read without an ECC error, a normal completion interrupt will be generated through Channel 0.

If a record is in error, it is flagged, and the operation is aborted with a channel 0 interrupt. At this time, the Header buffer contains the logical record number that is in error. A 'SECTOR NOT FOUND' error status will be returned.

It is assumed that the records read have sequential record numbers in them. This routine will skip a maximum of 66 headers in an attempt to locate record N+1.

3.6.14 Long Read, Op Code 0211

The Long Read command can read single or multiple sectors up to a maximum of 66 sectors without overlap. The controller supplies all 266 bytes of data as recorded on the disk for the particular sector specified and verifies ECC on the record. During a multiple sector Long Read, the second header read must be the previous record number plus one. If the second header read is not the previous record number plus one, the SECTOR NOT FOUND error bit is set and the operation will be aborted.

If an ECC error occurs during a Long Read of a particular sector or during a multiple sector operation, an interrupt is generated through channel 3 and the header bytes are properly updated. The read operation continues until either the last sector is reached or a fatal error occurs.

If DMA addresses need to be updated, the controller will generate the appropriate interrupt through channel 1. The controlling processor has 230 micrseconds to supply the updated pointer.

3.6.15 Long Write, Op Code 0212

The Long Write command can perform a single or multiple sector operation. This command writes header information from the header buffer and transfers 262 bytes of data into the specified record. The last 6 bytes written will be treated as the ECC data for the previous 256 bytes of data and 4 bytes of header written on the record. All other error checking and scattered DMA address restrictions are the same as a single or multiple sector Normal Write operation.

During this command, like a Normal Write command, at the end of each sector and upon receipt of channel 1 interrupt, the processor must furnish an updated header within 210 microseconds. If the updated header is not furnished within the allotted time period, the operation terminates with a channel 0 interrupt and a PARAMETER NOT SET status returned.

3.6.16 Controller Reset, Op Code 0216

The Controller Reset command unconditionally resets the controller's logic and is primarily used to abort multiple sector operations such as read, write, and read header and single sector operations such as read with error correction. No interrupt will be generated after the reset operation, and the controller will be made available for the next command.

3.6.17 Drive Reset, Op Code 0217

The Drive Reset command resets the heads of the requested drive, and clears both the seek error status (if present) and the head register. The controller remains busy for about 15 microseconds. A Seek Interrupt is generated when the drive has actually finished seeking. The maximum time needed for this interrupt to be generated is 800 microseconds.

3.6.18 Align Head, Op Code 0223

The Align Head command will turn on the read circuitry of a specified drive so that the physical head alignment may be performed on the 67 MB drive. This command will not cause a seek to any specific cylinder. A seek to the

proper cylinder should be performed prior to initiating this commmand. A controller reset command will abort the Align Head command and bring the disk controller to the idle mode for acceptance of a new command.

3.7 Interrupt Channels

Part of the peripheral control bus interface contains the logic for the generation of vectored interrupts. The controlling processor can monitor the interrupt conditions by reading the interrupt channels as described in the following subsections.

3.7.1 Channel 0 Interrupt

An interrupt is generated through this channel under two conditions:
- Fatal error
- Normal completion of all commands except SEEK.

3.7.2 Channel 1 Interrupt

An interrupt through this channel is generated only when the controller needs an updated DMA address and/or updated header information. The controlling processor must update the header/DMA address information within approximately 220 microseconds of this interrupt and set the parameter O.K. bit (Bit 7, Register 7, Port 0). If this bit is not set within the specified time, the present operation will be aborted with a channel 0 interrupt and the 'parameter not set' bit turned on in the Error Status buffer (Port 1, Register 2, Byte 2, Bit 7). A detailed description of the status bits can be found in Section 3.8.2.

3.7.3 Channel 2 Interrupt

An interrupt is generated through channel 2 when a seek is issued on a unit and the corresponding seek has been completed. The controlling processor has unconditional access to SEEK END status, which is updated periodically by the microcode. However, the SEEK END interrupt is generated only at specific times. Therefore, you may see a SEEK END status on a particular unit before the actual receipt of the SEEK END interrupt. If a SEEK END interrupt is generated, the corresponding SEEK END status will always be present.

If a seek is issued to a number of drives, and all of the drives finish seek at the same time, only one SEEK END interrupt will be generated.

3.7.4 Channel 3 Interrupt

Channel 3 interrupt is generated under two conditions:

- Occurrence of an ECC error during a multiple sector long read operation.
- Error free completion of the reading of every header during a multiple sector read header operation.

3.8 Disk Description

The following sections concern the format of the disk, the track error information, and the microcode.

3.8.1 Disk Format

	Field 1 Zeros Gap	Field 2 Sync	Field 3 Header	Field 4 Data	Field 6 ECC	Field 6 WG	Field 7 EOR GAP
Bytes	27	1	4	256	6	1	8

Field 1
Zeros Gap -- 27 bytes of zeros: 16 bytes for head skew and 11 bytes of Phase Locked Oscillator Sync

Field 2
Sync - one byte, octal 200 for synchronization of serial read data to the controller's logic

Field 3
Header - four bytes
The bit configuration for byte 0 is shown below:

Bit #

7	6	5	4	3	2	1	0
T	T	T	T	T	T	C9	C8

The bit configuration for byte 1 is shown below:

Bit#

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

The bit configuration for byte 2 is shown below:

Bit#7

7	6	5	4	3	2	1	0
T	T	T	D	H3	H2	H1	H0

Continued....

The bit configuration for byte 3 is shown below:

Bit#

7	6	5	4	3	2	1	0
0	S6	S5	S4	S3	S2	S1	S0

Where:
T = Track Error Information
Cx = Cylinder Address
Hx = Header Address
Sx = Sector Address
D = Drive Type

Field 4
Data - Total of 256 bytes

Field 5
ECC - Total of 6 bytes, standard Datapoint code

Field 6
WG - 1 byte of zeros as the write gate pad

Field 7
EOR Gap - 8 bytes of zeros as the end of record gap

3.8.2 Track Error Information

3.8.2.1 Register Contents Following an Error

For all error occurences (except parameter not set), the header buffer (Port 1, Register 4) 4th byte will contain the logical record number in which the posted error occurred. The error information bits in bytes 1 and 3 will be zeros. These error information bits will be shown as recorded on the disk surface only following a read header command with normal completion.

If the operation is aborted following a parameter not set error, the header buffer, last byte will contain the last record completed before the error was detected. At this time a channel 1 interrupt is generated. If the sector counter (Port 0, Register 4) is read within 230 microseconds of this interrupt, it will contain the physical sector corresponding to the returned logical sector number plus 1 if and only if the MSB bit of the sector counter is set.

The sector counter and the last byte of the header buffer bear no relationship other than as described above.

During Write 135 MB (Op code 0220), an interrupt for a parameter is generated as the target sector search continues. While writing the first sector, it is assumed that a valid parameter is given and no check is done at the microcode level to see if the parameter is given or not. During each subsequent sector however, the parameter OK bit is tested by the microcode using conventional protocol. Therefore, if a parameter is not sent following the first interrupt, one sector will be written with the sector address equal to the target sector and the parameter not set interrupt will be generated just prior to writing the second sector. In this case, the last byte of the header buffer returned will reflect the last header address written.

If the parameter was set by the running processor but came in late, then at the time of a parameter not set interrupt the parameter OK bit will still be set to indicate that the last parameter given was not accepted by the controller.

Whether the parameter OK bit set came in late or did not come in at all, the last header written by the controller can always be found by inspecting the last byte of the header buffer.

3.8.2.2 Register Contents Following Normal Completion

All registers will contain parameters related to the last completed sector. Plese note that the sector counter does not bear any direct relationship to the other registers except in the case of an error as noted above.

3.8.2.3 Track Error Format

The format of the track error information can be found by reading the first and third byte of any good sectors of a specified track. This information, once decoded, will tell you the number of defective sectors, if any, the order of the defective sectors (consecutive or non-consecutive) , and the drive type (67 MB or 135 MB) on which the error occured. If the defective sectors are scattered (non-consecutive), the error information will indicate the number of good sectors available from and including sectors 0 through 66. The figure below explains the meaning of each bit in the first and third header bytes of each track.

First Header Byte

T5	T4	T3	T2	T1	T0	C9	C8

Third Header Byte

T6	N2	N1	D	H3	H2	H1	H0

D = Drive type identifier (0 = 67 MB, 1 = 135 MB)

N2 N1
0 0 = no sectors in error
0 1 = one sector in error
1 1 = two consecutive sectors in error
1 0 = two non-consecutive sectors in error
C9, C8 = two MSB of cylinder number
Hx = head number
T0 through T5 = If the sectors in error are non-consecutive, these bits will indicate the number of available good sectors starting and including sector 0. Otherwise, these bits will be set to 0.
T6 = 1 to indicate entire track is defective

3.8.2.4 67 MB Drive Header Format

These drives are set at 64 sectors per track and the headers on all formatted records are as follows:

First Header Byte

1	1	0	0	0	0	C9	C8

Third Header Byte

0	0	0	0	0	H2	H1	H0

Where:
C9, C8 = two MSB of cylinder number
Hx = head number

3.8.2.5 Track Error Information in 135 MB Drive

135 MB drives are set at 66 sectors per track and the tracks may contain 0, 1, 2 or more defective sectors. Based on the physical position and number of errors in a track, headers are written using an offset mechanism that translates physical record numbers to logical record numbers.

The following describes all of the possible error cases that could occur:

Case 1:
Track with no error (header bytes are shown below):

Byte# \ Bit#	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	C9	C8
1	C7	C6	C5	C4	C3	C2	C1	C0
2	0	0	0	1	H3	H2	H1	H0
3	N7	N6	N5	N4	N3	N2	N1	N0

Where:
Nx = Logical Record Number

The 66 records are 0, 1, 2 ....., 077, 0376, 0377.
In the above track there is a 1 to 1 physical to logical addressing.

Case 2:
Track with 1 error in physical sector position 5 (decimal):
The bit configuration of the first and headers in this track is shown below:

First Header Byte

0	0	0	0	0	0	C9	C8

Third Header Byte

0	0	1	1	H3	H2	H1	H0

The physical records will look like the following:
074, 075, 076, 077, 0252, 0377, 0, 1, 2,....., 073

Case 3:
Track with 2 scattered (non-consecutive) defective sectors in position 4 and 12 (decimal):

First Header Byte

0	0	0	1	1	1	C9	C8

Third Header Byte

0	1	0	1	H3	H2	H1	H0

The physical records (numbers in octal) will look like the following:
075, 076, 077, 0252, 0, 1, 2, 3, 4, 5, 6, 0253, 7, 010, 011,....., 074

Case 4:
Track with 2 consecutive errors in physical sector position 5 and 6 (decimal):

First Header Byte

0	0	0	0	0	0	C9	C8

Third Header Byte

0	1	1	1	H3	H2	H1	H0

The physical sectors (numbers in octal) recorded will be the following:
074, 075, 076, 077, 0252, 0253, 0, 1, 2....., 073

Case 5:
Entire track is defective:
In this case all physical sectors will have record number 0252 (octal) in them.

3.8.3 Microcode Checks

A certain degree of intelligence is built in the microcode. Upon receiving a command the microcode will check the validity of supplied parameters for the following conditions:

-Disk unit number is less than or equal to 7
-Disk head number is less than 5 for the 67 MB drive or less than #11 for the 135 MB drive.
-Maximum number of sectors is less than or equal to 100 for the 67 MB drive and less than or equal to 102 for the 135 MB drive.

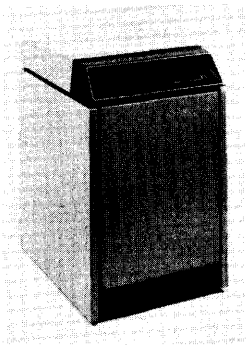
If any of the above conditions occur, operation is terminated immediately and a BOUNDARY ERROR status is returned.

All of the above tests will be bypassed if PORT 0, REG 1, BYTE 3 is written non-zero. Byte 3 should be written as zero for a drive with non-standard configuration.

3.8.3.1 Microcode Fields

Below is a list of the microcode fields containing the bit location and a brief description of the function of each field.

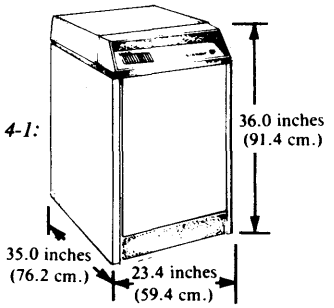
Bits	Description
0 - 9	Immediate field
10 - 11	Port select on register files
12 - 15	Bus destination / ALU destination (register)
16	Destination control field, bit equal to one if ALU selected
17 - 20	Bus source / ALU source (register)
21	Source select, bit equal to one if source is ALU
22 - 25	Independent action code
26 - 29	Condition code
30 - 32	ALU operation code
33 - 35	ALU function
36	Carry
37 - 39	ALU operation destination
44 - 47	Spare



4.0 Physical Description

Disk Drive Cabinet Dimensions
Width: 23.4 inches (59.4 cm.)
Height: 36.0 inches (91.4 cm.)
Depth: 35.0 inches (76.2 cm.)
Weight: 450 pounds

Figure 4-1:



5.0 Environmental Requirements

Temperature: 50 to 100 degrees F (10 to 38 C)
Humidity: 20 to 90% relative, non-condensing
Heat Dissipation:
67 MB 2990 BTU/Hour
135 MB 2400 BTU/Hour

6.0 Interface Requirements

6.1 Cable A Connector Pin Assignments

Signal Name	Flat Cable Pin Polarity Lo (-) / Hi(+)		Source
Unit Select Tag	22	52	Controller
Unit Select 1	23	53	Controller
Unit Select 2	24	54	Controller
Unit Select 4	26	56	Controller
Unit Select 8	27	57	Controller
Tag 1	1	31	Controller
Tag 2	2	32	Controller
Tag 3	3	33	Controller
Bit 0	4	34	Controller
Bit 1	5	35	Controller
Bit 2	6	36	Controller
Bit 3	7	37	Controller
Bit 4	8	38	Controller
Bit 5	9	39	Controller
Bit 6	10	40	Controller
Bit 7	11	41	Controller
Bit 8	12	42	Controller
Bit 9	13	43	Controller
Open Cable Detector	14	48	Controller
Index	18	48	Drive
Sector	25	55	Drive

Continued....

Signal Name	Flat Cable Pin Polarity Lo (-) / Hi (+)		Source
Fault	15	45	Drive
Seek Error	18	48	Drive
On Cylinder	17	47	Drive
Unit Ready	19	49	Drive
Address Maark Found	20	50	Drive
Write Protected	8	58	Drive
Power Sequence Pick		29	Controller
Power Sequence Hold		59	Controller
Busy	21	51	Drive
Not Used (Spare)	30	60	

6.2 B Cable Conector Pin Assignments

Signal Name	Flat Cable Pin Polarity Lo (-)/Hi (+)		Source
Write Data	8	20	Controller
Ground	7		
Write Clock	6	19	Controller
Ground	18		
Servo Clock	2	14	Drive
Ground	1		
Read Data	3	16	Drive
Ground	15		
Read Clock	5	17	Drive
Ground	4		
Seek End	10	23	Drive
Unit Selected	22	9	Drive
Ground	21	23	
Ground	11		
Ground	25		

6.3 Primary AC Power

120 VAC (+8 or -18 VAC), 60 Hz (+0.6 or 1.0 Hz)
220 VAC 50 Hz (+15 or -25 VAC), 50 Hz (+0.5 or -1.0 Hz)
240 VAC 50 Hz (+17 or -27 VAC), 50 Hz (+0.5 or -1.0 Hz)

7.0 Options

7.1 230 VAC Option

Factory-installed option 9372 is available for all of the disk drives providing operation from 230 VAC (see Section 6.3). With this option complete model codes for the disk drives are:

9395/9372 - Dual Disk Drive (67 MB/135 MB) in cabinet, 230 VAC
9397/9372 - Dual Disk Drive (67 MB/ 135 MB) in cabinet, IMOD, 230 VAC
9331/9372 - Single Disk Drive (135 MB) in cabinet, 230 VAC
9332/9372 - Dual Disk Drive (135 MB/135 MB) in cabinet, 230 VAC
9333/9372 - Expansion Drive (135 MB) without cabinet, 230 VAC

8.0 Shipping List

The following items are shipped with the 67/135 MB Disk Drives:

Quantity	Item
1	Disk System (9395, 9397, 9331, 9332, 9333)
1	67 MB/135 MB Product Specification (Document No. 61014)

NOTE: This shipping list is offered for information only and may be amended from time to time by Datapoint Corporation.

DATAPOINT

Datapoint recommends that its customers use Datapoint Customer Supplies. These disks, diskettes, cassettes and ribbons are certified by Datapoint to meet all Datapoint hardware specifications for consistent optimum performance. Reference Document No. 80000, the Customer Supplies Catalog, for ordering information.